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EXAMINER

FLETCHER, JAMES A

ART UNIT	PAPER NUMBER
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2621

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/380,187

Applicant(s)

YAMAGUCHI ET AL.

Examiner

James A. Fletcher

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 12-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. This action vacates the previous final rejection dated 10 August 2005 in view of the amendment filed 13 June 2005, and addresses issues raised in the Appeal Brief filed 30 May 2006, and the Request for Reconsideration dated 7 November 2006.
2. Applicant's arguments with respect to claims 1-7, 10, and 12-17 have been considered but are moot in view of the new ground(s) of rejection.
3. Applicant's arguments filed 13 June 2005 with respect to claims 8-9 and 18 have been fully considered but they are not persuasive.

In re page 16, Applicant's Representative states: "while Yanagihara disclose the ability to add padding data to a source packet in order to convert an MPEG-PS data pack of 2,048 bytes into isochronous communication packets that can be transmitted in accordance with the IEEE 1394 standard, Applicants respectfully submit that the padding of Yanagihara is not added so as to equalize the bus width of a pipeline transfer, as recited in claim 8."

The Examiner respectfully disagrees. In the applicant's specification, page 37, lines 15-17, the addition of a sufficient amount of padding data to make the pack an appropriate size will read on the recited "becomes equal to the bus width of pipeline transfer." This justifies the Examiner's interpretation of Yanagihara Col 7, lines 1-7 as padding the data for identical purposes to the Applicant's recitation.

In re page 17, Applicant's Representative states: "Applicants respectfully submit, however, that Yanagihara does not disclose the ability to insert a specific code

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sequence in the last packet in a packet sequence, wherein the formatter is operable to add a predetermined number of pseudo data to the rear of the specific code sequence, as recited in claim 9.”

The Examiner respectfully disagrees. Although the Applicant's Representative has not clearly stated where he believes Yanagihara to be deficient, the Examiner will attempt to address the various elements of his statement. As noted in the non-final rejection and taken as a whole, Yanagihara discloses the ability to insert a specific code sequence in the last packet in a packet sequence (Col 13, line 67 – Col 14, line 1 “add 28-byte padding data to the hindmost end of each source packet”), wherein the formatter is operable to add a predetermined number (Col 7, lines 1-4 “the packeting circuit 45...adds 124-byte padding data to the time stamp and the 2,048 byte pack in order that the total byte length be a multiple of 16) of pseudo data (Col 7, line 5 “As padding data, no particular information is held”) to the rear of the specific code sequence (Col 13, line 67 – Col 14 as recited above).

In re page 2 of remarks submitted 7 November 2006, Applicant's Representative states: “col. 10, lines 51-56 of Fujinami is in the Brief Description of the Drawings section of the reference and merely provides a general description of Figs. 2-4 and in no way whatsoever relates to a CIT header as discussed in the Office Action.

The Examiner acknowledges his error in not properly referencing Yanagihara et al, a reference provided to the Applicants previously, as a combined reference in his rejection of claim 1.

In re page 5 of remarks submitted 7 November 2006, Applicant's

Representative states: "Applicants submit that the control circuit 24 cannot correspond to both of a matching status information outputter that outputs matching status information and a data formatter that outputs predetermined data in accordance with matching status information."

The Examiner respectfully notes that he already declared this argument moot in light of the new grounds of rejection, that being the inclusion of Yanagihara's explicit teaching of an output matching the status information at a head part of the packet start code.

In re page 8 of remarks submitted 7 November 2006, Applicant's

Representative states: "Yanagihara does not disclose, suggest, or otherwise render obvious the feature of a formatter that is operable to add a predetermined number of pseudo data to the rear of a code sequence indicating the end of the coded data so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data, as recited in claim 8"

The Examiner respectfully disagrees. The term "pipeline," as used by the applicant is a broad term, encompassing virtually any element of a transmission channel. The addition of padding data to make the packets conform to an IEEE 1395 "pipeline" is explicitly disclosed by Yanagihara, as analyzed and discussed in the previous office action.

Claim Rejections - 35 USC § 102

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4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 8, 9, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagihara et al (6,172,989).

Regarding claim 8, Yanagihara et al disclose a coded signal reproduction apparatus comprising:

- an end code sequence detector operable to detect, from code sequences of coded data, a code sequence indicating the end of the coded data (Col 1, lines 66-67 “The packet header is formed of ‘Data_Length’ at representing the data length”); and
- formatter operable to add a predetermined number of pseudo data to the rear of the code sequence indicating the end of the coded data (Col 7, lines 1-5 “the packeting circuit 45 sets the supplied time information as a 4-byte time stamp and adds 124 byte padding data to the time stamp and the 2,048 byte pack in order that the total byte length be a multiple of 16, as shown in FIG.4”)/. so that the data bus width of pipeline transfer including the end of the coded data becomes equal to the bus width of pipeline transfer including other data (Col 8, lines 19-20 “if the playback rate is changed, FN and DB are changed in accordance”), when a code sequence indicating the end of the code data is detected by the end code sequence detector (Col 13, line 66 -

Col 14, line 3 "The process then advances to step S3 to add 28-byte padding data to the hindmost end of each source packet in order to form data blocks of the quadlet unit size").

Regarding claim 9, Yanagihara et al disclose a coded signal reproduction apparatus comprising:

- a specific code sequence inserter operable to insert a specific code sequence in the last packet in a packet sequence before decoding;
- wherein the formatter is operable to add a predetermined number of pseudo data to the rear of the specific code sequence (Col 9, line 66- Col 10, line 1 "The packeting circuit 45...first adds padding data to a pack of 2,048 bytes, as shown in FIG. 10." Fig. 10 clearly shows the padding data added to the end of the sequence).

Regarding claim 18, Yanagihara et al disclose a coded signal reproduction apparatus wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed (Col 5, lines 9-13 "The demultiplexer 13 is arranged to sort, out of supplied MPEG-PS data, a video pack having video information, an audio pack having audio information, and a sub picture pack having information such as captions, and to output the packs to a decoding section").

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-3 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujinami et al (5,568,274), in further view of Yanagihara et al.

Regarding claim 1, Fujinami et al disclose a coded signal reproduction apparatus comprising:

- matching status information outputter operable to detect the matching status of a code (Col 3, lines 17-22 "The control circuit 21 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream_ID of the packet header received from the header separation circuit 22") which is input for every predetermined bit with a prefix code of a packet start codes (Col 2, lines 1-2 "Each packet includes a header which includes a Packet_Start_Code_Prefix"),; and
- a data formatter operable to output predetermined data in accordance with the matching status information (Col 3, lines 17-22 "The control circuit 21 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream_ID of the packet header received from the header separation circuit 22") when the code is judged not to be a part of the packet start code (Col 3, lines 9-12 "the header separation circuit 22 in the separation circuit 21 separates pack headers and packet headers from the multiplexed signal read

out from the DSM 10” and Col 15, lines 29-33 “The control circuit 24 of the separation circuit 21 causes the switching circuit 23 to connect the input terminal G successively to the output terminals H1 and H2 in accordance with the stream_ID of the packet header received from the header separation circuit 22”);

- wherein, when a next packet start code is recognized, the predetermined data is output so as to be positioned at a head part of the data other than a header which follows the next packet start code (Col 8, lines 64-67 “The signal-type marker is located adjacent to the signal portion of the predetermined type to indicate the signal portion of the predetermined type in the multiplexed signal”).

Fujinami et al disclose outputting matching status information to a control switch as discussed above, but do not disclose a predetermined data at a head part of the packet start code.

Yanagihara et al teach placing predetermined data at the head part of the packet start code (Col 10, lines 56-51 “In this CIP header, if MPEG-PS data is transmitted [that is, if the value in the FMT area is 100100 [binary]], the logarithm of the second number of fractions FN_2 to base 2 [$\log_2 [FN_2]$] is written in the FN area, and the value in the original [FIG. 26] QPC area [the 19th to 21st bits of the No. 0 quadlet] is fixed at 0”).

As taught by Yanagihara, the placement of data to be used for the decoding of a packet at the head of the packet is widely known and commercially

available, providing the decoder with information at a time when it is most useful, and reducing the amount of memory required to store such data.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Fujinami et al in order to provide for insertion of matching status information at the head part of a packet start code.

Regarding claims 2 and 3, Fujinami et al disclose a coded signal reproduction apparatus wherein the matching status information outputter includes:

- a head code detection unit operable to detect the matching status of the head part of the packet start code at every predetermined bit from the input code sequence, and to output matching information at the present point of time (Col 3, lines 7-9 “The multiplexed signal...is reproduced and decoded by the reproducing apparatus” and lines 12-15 “The header separation circuit 22 supplies the headers to the control circuit 24, and supplies the multiplexed signal to the input terminal G of the switching circuit 23”); and
- a matching status historical information hold unit for operable to receive the matching information at the present point of time, and to hold historical information of the matching status of the head code (Col 15, lines 22-24 “The control circuit 24 supplies each entry point it receives from the header separation circuit 22 to the entry point storage device 41, where it is stored”); and
- start code discriminator operable to discriminate the packet start code by using the historical information (Col 15, lines 24-28 “Since the current read

position is supplied from the drive apparatus 10 to the control circuit 24, the control circuit 24 can store the position and the contents of each entry point in a corresponding relationship to each other”) and a packet start code identifier existing in the later half part of the packet start code (Fig 3 shows a packet header ID following a packet start code prefix).

Regarding claims 10 and 12-13, Fujinami et al disclose a coded signal reproduction apparatus wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed (Fig 13 shows audio and video signals multiplexed into a data stream, and Fig 14 shows several reproduction information data in the same stream).

8. Claims 8, 9 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagihara et al (6,172,989).

9. Claims 4, 6-7, 14, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujinami et al as applied to claims above, and further in view of Boden (5,633,686).

Regarding claim 4, Fujinami et al disclose a coded signal reproduction apparatus wherein the matching status information outputter includes:

- a head code detection unit operable to detect the matching status of the head part of the packet start code at every predetermined bit from the input code sequence, and to output matching information at the present point of time (Col 3, lines 7-9 “The multiplexed signal...is reproduced and decoded by the reproducing apparatus” and lines 12-15 “The header separation circuit 22

supplies the headers to the control circuit 24, and supplies the multiplexed signal to the input terminal G of the switching circuit 23"); and

- a matching status historical information hold unit operable to receive the matching information at the present point of time, and to hold historical information of the matching status of the head code (Col 3, lines 17-22 "The control circuit 24 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output terminals H1 and H2 in accordance with the stream_ID of the packet header received from the header separation circuit 22." In order for a full packet to be steered to the appropriate decoder, the header information must be stored in the control of the switching circuit.)

Fujinami et al do not specifically disclose a start code discrimination unit operable to discriminate a hierarchy start code of video data in accordance with the historical information and a video hierarchy identifier of coded video data which exists in a position corresponding to the latter half of the packet start code.

Boden teaches a start code discrimination unit operable to discriminate a hierarchy start code of video data in accordance with the historical information (Col 7, lines 10-23 "the controller starts writing the video information to the memory array...until the maximum programmed address is reached...The write bank controller selects the next bank of memory into which data is to be written") and a video hierarchy identifier of coded video data which exists in a position corresponding to the latter half of the packet start code (Col 8, lines 12-13 "the

decoder awaits reception of the thirty-two bit start code” and Col 8, lines 18 -19 “Following the start code, the next two bytes received are the system data and system control bytes”).

As taught by Boden, basing a code hierarchy on historical information is a useful and easily used technique of gathering the data required for generating the hierarch, and placing such additional data towards the end of the data area used for such information does not require the rearrangement of existing data.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Fujinami et al in order to base hierarchy data on historical information, and to place that data in the second half of the area in which it logically belongs.

Regarding claim 6, Fujinami et al disclose a coded signal apparatus wherein the header analyzer includes a header analysis unit operable to analyze the header of the packet and to output the reproduction information (Fig 17, item 67, “Control Circuit”), and a reproduction information hold unit operable to hold the reproduction information (Fig 17, item 93 “Entry Point Storage Device” and item 68 “TOC Storage Device”).

Regarding claim 7, Fujinami et al disclose a coded signal reproduction apparatus wherein the header analyzer is operable to activate when the start code is identified (Col 12, lines 20-21 “The pack begins with a Pack_Header consisting of a Pack_Start_Code” and Col 3, lines 17-22 “The control circuit 21 in the separation circuit 21 successively connects the input terminal G of the switching circuit 23 to the output

terminals H1 and H2 in accordance with the stream_ID of the packet header received from the header separation circuit 22”).

Regarding claims 14, 16, and 17, Fujinami et al disclose a coded signal reproduction apparatus wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed (Fig 13 shows audio and video signals multiplexed into a data stream, and Fig 14 shows several reproduction information data in the same stream).

10. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujinami et al as applied to claims above, and further in view of Toyohara (5,768,265).

Regarding claim 5, Fujinami et al disclose a coded signal reproduction apparatus comprising:

- header analyzer operable to analyze the header of the packet to output reproduction information when the input code sequence is coded video data (Col 3, lines 12-15 “The header separation circuit 22 supplies the headers to the control circuit 24, and supplies the multiplexed signal to the input terminal G of the switching circuit 23”).

Fujinami et al are silent on the topic of effectiveness of the data.

Toyohara teaches a data format means that inserts the reproduction information together with information indicating effectiveness of the reproduction information, in a predetermined position in the decoded video data (Col 8, lines 39-41 “the identifier discriminating circuit 410 analyses the identifier attached to the respective data to identify the effectiveness of the data”).

As taught by Toyohara, effectiveness data lessens the burden on the processor by identifying packets that need not be decoded.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Fujinami et al in order to provide effectiveness data to the decoder.

Regarding claim 15, Fujinami et al disclose a coded signal reproduction apparatus wherein the input code sequence is a coded and multiplexed signal in which audio, video, and reproduction information annexed thereto are multiplexed (Fig 13 shows audio and video signals multiplexed into a data stream, and Fig 14 shows several reproduction information data in the same stream).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Fletcher whose telephone number is (571) 272-7377. The examiner can normally be reached on 7:45-5:45 M-Th, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on (571) 272-7950. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAF
24 November 2006


James J. Groody
Supervisory Patent Examiner
Art Unit 262-2621